AMENDMENTS TO THE CLAIMS

Claims 1-28. (Canceled)

29. (Previously presented) A semiconductor device comprising:

a substrate;

an insulating layer provided over said substrate;

an electropolished patterned metal layer provided within an opening of said insulating layer, wherein said electropolished metal layer has a thickness of approximately 50 to 300 Angstroms and wherein a top surface of said electropolished metal layer is electropolished down to said insulating layer so that said top surface of said electropolished metal layer is at the same level with a top surface of said insulating layer; and

a photoresist plug provided within said opening and over and in contact with said electropolished patterned metal layer.

30. (Original) The semiconductor device of claim 29, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

31. (Original) The semiconductor device of claim 29, wherein said electropolished patterned metal layer contains a noble metal.

32. (Original) The semiconductor device of claim 31, wherein said electropolished patterned metal layer is a platinum layer.

Claim 33. (Canceled)

34. (Previously presented) The semiconductor device of claim 29, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

35. (Original) The semiconductor device of claim 29, wherein said electropolished patterned metal layer forms a lower capacitor electrode of said semiconductor device.

36. (Previously presented) A memory cell comprising:

a transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate;

an electropolished patterned metal layer within an insulating layer provided over said substrate, said electropolished patterned metal layer having a thickness of about 50 to about 300 Angstroms; and

a container capacitor including a lower electrode, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode, and said dielectric layer being in contact with said insulating layer.

37. (Original) The memory cell of claim 36, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

38. (Original) The memory cell of claim 37, wherein said electropolished patterned metal layer contains a noble metal.

39. (Original) The memory cell of claim 38, wherein said electropolished patterned metal layer is a platinum layer.

Claim 40. (Canceled)

41. (Previously presented) The memory cell of claim 36, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

Claim 42. (Canceled)

Claim 43. (Canceled)

44. (Currently amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising a container capacitor provided within an insulating layer, said container capacitor including a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer, said upper electrode comprising doped polysilicon.

45. (Original) The processor-based system of claim 44, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

46. (Original) The processor-based system of claim 45, wherein said electropolished patterned metal layer contains a noble metal.

47. (Original) The processor-based system of claim 46, wherein said electropolished patterned metal layer is a platinum layer.

Claim 48. (Canceled)

49. (Original) The processor-based system of claim 44, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

Claim 50. (Canceled)

51. (Original) The processor-based system of claim 44, wherein said integrated circuit is a memory module.

52. (Original) The processor-based system of claim 51, wherein said memory module is a DRAM memory.

53. (Original) The processor-based system of claim 51, wherein said memory module is a SRAM memory.

54. (Original) The processor-based system of claim 51, wherein said memory module is a MCM memory.

55. (Previously presented) A container capacitor comprising:

a lower electrode provided within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom;

a second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer; and

an upper electrode provided over said second insulating layer.

56. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

57. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer has a thickness of approximately 50 to 300 Angstroms.

58. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

59. (Currently amended) A container capacitor provided within an opening of an insulating layer of a substrate comprising:

a tantalum nitride barrier conductive layer provided at a bottom of said opening;

a lower electrode provided over said tantalum nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom, said lower electrode having a thickness of approximately 100 Angstroms;

a dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer; and

an upper electrode <u>comprising doped polysilicon</u> provided over said dielectric material and wherein said lower electrode, said dielectric material and said upper electrode form a container capacitor.

60. (Previously presented) A container capacitor structure comprising:

an insulating layer provided over a substrate;

a plurality of rectangular openings provided in said insulating layer;

a plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said rectangular openings, said lower electrodes being formed as discrete electropolished metal layers; and

a dielectric layer associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer.

61. (Previously presented) The capacitor structure of claim 60, wherein said capacitor structure further comprises an upper electrode associated with each of said discrete lower electrodes.

62. (Previously presented) The capacitor structure of claim 60, wherein said electropolished lower capacitor electrodes have a thickness of approximately 50 to 300 Angstroms.

63. (Previously presented) The capacitor structure of claim 62, wherein said lower capacitor electrodes have a thickness of approximately 100 Angstroms.

64. (Previously presented) The capacitor structure of claim 60, wherein said lower capacitor electrodes contain platinum.